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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/759,666	01/13/2001	Hiroaki Tsugane	15.29/5629	2708

7590 12/28/2004

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EXAMINER	
SCHILLINGER, LAURA M	

ART UNIT	PAPER NUMBER
2813	

DATE MAILED: 12/28/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/759,666	TSUGANE ET AL.	
	Examiner	Art Unit	
	Laura M. Schillinger	2813	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *13 October 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *2-4,6,8,16,19-23 and 27-29* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *3* is/are allowed.

6)☒ Claim(s) *2,16,19,20 and 29* is/are rejected.

7)☒ Claim(s) *4,6,8,21-23,27 and 28* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

Applicant's arguments with respect to the Examiner's restriction requirement are deemed persuasive. Consequently, the restriction requirement is withdrawn.

Claim Objections

Claims 4, 6, 8, 21-23, and 27-28 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claim Rejections - 35 USC § 112

Claim 29 is rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. The specification does not teach to form a silicon nitride layer and then oxidize a portion of it.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 2 and 16 are rejected under 35 U.S.C. 102(e) as being anticipated by Koo et al ('446).

Koo teaches the following claimed limitations as recited below:

2. (previously presented) A method for manufacturing a semiconductor device, the semiconductor device having a DRAM including a first capacitor formed in a DRAM region of a semiconductor substrate, and a second capacitor formed in an analog element region of the semiconductor substrate, the method comprising the steps of:

(a) simultaneously forming a storage node of the first capacitor and a lower electrode of the second capacitor (Col.2, lines: 10-25);

(b) simultaneously forming a dielectric layer of the first capacitor and a dielectric layer of the second capacitor (Col.2, lines: 10-25);

(c) simultaneously forming a cell plate of the first capacitor and an upper electrode of the second capacitor(Col.2, lines: 10-25); and

before the step (a), the step of simultaneously forming a word line that is a component of the DRAM and a connection layer that is located in a common layer of the word line (is the connector from the plug to the source/drain region of the CMOS) and that electrically connects the lower electrode to another element in the semiconductor device (Col.6, lines: 43-52).

16. (previously presented) A method for manufacturing a semiconductor device, the semiconductor device having a DRAM including a first capacitor formed in a DRAM region of a semiconductor substrate, and a second capacitor formed in an analog element region of the semiconductor substrate, the method comprising:

forming a first conducting layer and etching a portion of the first conducting layer to form a storage node of the first capacitor and a lower electrode of the second capacitor (Col.2, lines: 10-25);

forming a dielectric layer and etching a portion of the dielectric layer to form a dielectric layer region of the first capacitor and a dielectric layer region of the second capacitor (Col.2, lines: 10-25);

forming a second conducting layer and etching a portion of the second conducting layer to form a cell plate of the first capacitor and an upper electrode of the second capacitor (Col.,2 lines: 10-25); and prior to forming the storage node of the first capacitor and the lower electrode of the second capacitor, forming an additional conducting layer and etching the additional conducting layer to form a word line that is a component of the

DRAM and to form a connection layer that is located in a common layer of the word line and that is configured to electrically connect the lower electrode to another element in the semiconductor device (Col.6, lines: 43-52).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 19-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Koo et al ('446), and further in view of Takada et al.

In reference to claim 19, Koo teaches a method comprising:

forming a first conducting layer and etching a portion of the first conducting layer to form a storage node of the first capacitor and a lower electrode of the second capacitor (Col.2, lines: 10-25);

forming a dielectric layer and etching a portion of the dielectric layer to form a dielectric layer region of the first capacitor and a dielectric layer region of the second capacitor (Col.2, lines: 10-25); and

However fails to teach Applicant's additional claimed limitation of:

forming a second conducting layer and etching a portion of the second conducting layer to form a cell plate of the first capacitor and an upper electrode of the second capacitor; wherein the etching a portion of the second conducting layer also forms a first resistance element and a second resistance element in the analog element region.

However, Takada et al ('772) teaches a similar method including forming a second conducting layer and etching a portion of the second conducting layer to form a cell plate of the first capacitor and an upper electrode of the second capacitor; wherein the etching a portion of the second conducting layer also forms a first resistance element and a second resistance element in the analog element region (Col.11, lines: 10-15 and 25-35).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Koo's teachings to further include a forming simultaneously a first and second resistance element with the cell plate of the first and second capacitors, because as Takada teaches, the first and second resistance elements may be formed simultaneously with the upper electrode (cell plate) of a single capacitor (Col.11, lines: 10-15 and 25-35). Therefore it would be an obvious modification to form two upper electrodes for two capacitors as taught by Koo in combination with Takada's simultaneous formation of two resistance elements formed simultaneously with a single upper electrode because is it requires merely a repetition of parts.

20. (previously presented) A method as in claim 19, further comprising performing at least one ion-implantation of an impurity into part of the second conducting layer prior to the etching a portion of the second conducting layer (Takada-Col.11, lines: 25-35).

Allowable Subject Matter

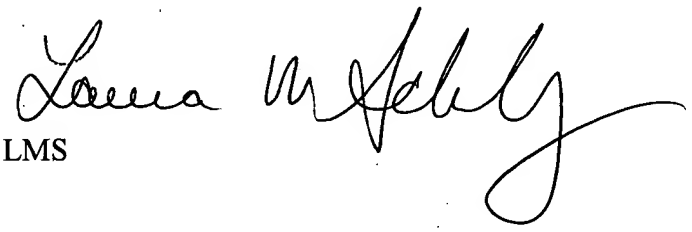
The following is a statement of reasons for the indication of allowable subject matter: In reference to claims 3,4,6,8, 21-23 prior art fails to teach in combination with other recited claimed limitations, a first and second resistance element formed in an analog region with the first resistance element having a different resistance value from the second as a result of impurity diffusion/implantation or silicide materials. Although Takada teaches that it is possible to vary resistance by implantation or diffusion, Takada does not teach to vary one resistance element with respect to the other. Claims 3-4, 6,8, and 21-23 all contain such allowable subject matter. Furthermore, prior art fails to teach in combination the limitations of claims 27 and 19, that is the silicide layer in direct contact with an upper surface of the first resistance element and forming an oxide layer in direct contact with an upper surface of the second resistance element. Claim 28 depends from claim 27 and therefore also contains allowable subject matter.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Laura M. Schillinger whose telephone number is (571) 272-1697. The examiner can normally be reached on M-T, R-F 7:00-5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Carl W. Whitehead, Jr. can be reached on (571) 272-1702. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



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